

EAST Search History

| Ref # | Hits | Search Query | DBs | Default Operator | Plurals | Time Stamp |
|-------|-------|--|--|------------------|---------|------------------|
| L1 | 86 | ("4814981" "5251311" "5355487" "5386565" "5423050" "5434804" "5440705" "5448576" "5452432" "5455936" "5479652" "5483518" "5488688" "5513317" "5530965" "5570375" "5590354" "5596734" "5598551" "5608881" "5613153" "5625785" "5627842" "5657273" "5659679" "5682545" "5704034" "5708773" "5724505" "5724549" "5737516" "5751621" "5768152" "5771240" "5774701" "5778237" "5781558" "5796978" "5809293" "5828825" "5832248" "5835963" "5848247" "5848264" "5860127" "5862387" "5867726" "5884023" "5884092" "5896550" "5918045" "5930523" "5930833" "5938778" "5943498" "5944841" "5950012" "5953538" "5956477" "5964893" "5978874" "5978902" "5983017" "5983366" "5983379" "5996092" "5999112" "6035422" "6094729" "6108761" "6142683" "6145099" "6145123" "6148381" "6154857" "6167499" "6167536" "6175914" "6185732" "6189140" "6243836" "6269454" "6282701" "6314530" "6345295" "6370660").PN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2006/05/08 12:22 |
| L2 | 17 | L1 and compress\$4 | US-PGPUB; USPAT; EPO; DERWENT | OR | OFF | 2006/05/08 12:22 |
| L3 | 17 | L2 and @ad<"20010303" | US-PGPUB; USPAT; EPO; DERWENT | OR | OFF | 2006/05/08 12:28 |
| L4 | 21293 | trace and compress\$4 and @ad<"20010303" | US-PGPUB; USPAT; EPO; DERWENT | OR | OFF | 2006/05/08 14:40 |

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|-----|------|--|-------------------------------|----|-----|------------------|
| L5 | 5120 | trace and compress\$4 and ((integrated adj circuit) or processor or chip) and @ad<"20010303" | US-PGPUB; USPAT; EPO; DERWENT | OR | OFF | 2006/05/08 12:29 |
| L6 | 923 | trace and packet\$1 and compress\$4 and ((integrated adj circuit) or processor or chip) and @ad<"20010303" | US-PGPUB; USPAT; EPO; DERWENT | OR | OFF | 2006/05/08 12:30 |
| L7 | 69 | trace and packet\$7 and debug\$4 and @ad>"20000401" and @ad<"20010303" and compress\$4 | US-PGPUB; USPAT; EPO; DERWENT | OR | OFF | 2006/05/08 14:29 |
| L9 | 179 | 708/203.ccls. and @ad<"20010303" | US-PGPUB; USPAT; EPO; DERWENT | OR | OFF | 2006/05/08 14:34 |
| L10 | 86 | (trace near compress\$4) and @ad<"20010303" | US-PGPUB; USPAT; EPO; DERWENT | OR | OFF | 2006/05/08 14:54 |
| L11 | 344 | 709/247.ccls. and @ad<"20010303" | US-PGPUB; USPAT; EPO; DERWENT | OR | OFF | 2006/05/08 15:13 |
| L12 | 146 | 341/76.ccls. and @ad<"20010303" | US-PGPUB; USPAT; EPO; DERWENT | OR | OFF | 2006/05/08 15:35 |
| L13 | 0 | trace near compress\$4 and @ad<"20010303" | IBM_TDB | OR | OFF | 2006/05/08 15:35 |
| S1 | 15 | 703/24.ccls. and @pd>"20051201" | US-PGPUB; USPAT; EPO; DERWENT | OR | OFF | 2006/05/07 16:20 |
| S2 | 22 | 714/45.ccls. and @pd>"20051201" | US-PGPUB; USPAT; EPO; DERWENT | OR | OFF | 2006/05/07 16:25 |
| S4 | 103 | 714/724.ccls. and @pd>"20051201" | US-PGPUB; USPAT; EPO; DERWENT | OR | OFF | 2006/05/07 16:44 |
| S6 | 6 | trace and packet\$7 and debug\$4 and ((integrated adj circuit) or processor) and @ad<"20000401" and @pd>"20051201" | US-PGPUB; USPAT; EPO; DERWENT | OR | OFF | 2006/05/07 16:59 |

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| S8 | 225 | trace and packet\$7 and debug\$4 and (chip) and @ad<"20000401" | US-PGPUB; USPAT; EPO; DERWENT | OR | OFF | 2006/05/07 16:48 |
| S9 | 249 | trace and packet\$7 and debug\$4 and @ad<"20000401" and compress\$4 | US-PGPUB; USPAT; EPO; DERWENT | OR | OFF | 2006/05/08 14:25 |
| S10 | 86 | ("4814981" "5251311" "5355487" "5386565" "5423050" "5434804" "5440705" "5448576" "5452432" "5455936" "5479652" "5483518" "5488688" "5513317" "5530965" "5570375" "5590354" "5596734" "5598551" "5608881" "5613153" "5625785" "5627842" "5657273" "5659679" "5682545" "5704034" "5708773" "5724505" "5724549" "5737516" "5751621" "5768152" "5771240" "5774701" "5778237" "5781558" "5796978" "5809293" "5828825" "5832248" "5835963" "5848247" "5848264" "5860127" "5862387" "5867726" "5884023" "5884092" "5896550" "5918045" "5930523" "5930833" "5938778" "5943498" "5944841" "5950012" "5953538" "5956477" "5964893" "5978874" "5978902" "5983017" "5983366" "5983379" "5996092" "5999112" "6035422" "6094729" "6108761" "6142683" "6145099" "6145123" "6148381" "6154857" "6167499" "6167536" "6175914" "6185732" "6189140" "6243836" "6269454" "6282701" "6314530" "6345295" "6370660").PN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2006/05/08 09:53 |

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|-----|----|--|--|----|-----|------------------|
| S11 | 86 | ("4814981" "5251311" "5355487" "5386565" "5423050" "5434804" "5440705" "5448576" "5452432" "5455936" "5479652" "5483518" "5488688" "5513317" "5530965" "5570375" "5590354" "5596734" "5598551" "5608881" "5613153" "5625785" "5627842" "5657273" "5659679" "5682545" "5704034" "5708773" "5724505" "5724549" "5737516" "5751621" "5768152" "5771240" "5774701" "5778237" "5781558" "5796978" "5809293" "5828825" "5832248" "5835963" "5848247" "5848264" "5860127" "5862387" "5867726" "5884023" "5884092" "5896550" "5918045" "5930523" "5930833" "5938778" "5943498" "5944841" "5950012" "5953538" "5956477" "5964893" "5978874" "5978902" "5983017" "5983366" "5983379" "5996092" "5999112" "6035422" "6094729" "6108761" "6142683" "6145099" "6145123" "6148381" "6154857" "6167499" "6167536" "6175914" "6185732" "6189140" "6243836" "6269454" "6282701" "6314530" "6345295" "6370660").PN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2006/05/08 09:53 |
| S12 | 17 | S11 and compress\$4 | US-PGPUB; USPAT; EPO; DERWENT | OR | OFF | 2006/05/08 12:22 |
| S14 | 2 | "20010034597".pn. | US-PGPUB; USPAT; EPO; DERWENT | OR | OFF | 2006/05/08 10:57 |

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Laha, S.; Patel, J.H.; Iyer, R.K.;
Computers, IEEE Transactions on
Volume 37, Issue 11, Nov. 1988 Page(s):1325 - 1336
Digital Object Identifier 10.1109/12.8699
[Abstract](#) | Full Text: [PDF\(944 KB\)](#) [IEEE JNL](#)
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 2. **Address tracing for parallel machines**

Stunkel, C.B.; Janssens, B.; Fuchs, W.K.;
Computer
Volume 24, Issue 1, Jan. 1991 Page(s):31 - 38
Digital Object Identifier 10.1109/2.67191
[Abstract](#) | Full Text: [PDF\(628 KB\)](#) [IEEE JNL](#)
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 3. **Efficient program tracing**

Larus, J.R.;
Computer
Volume 26, Issue 5, May 1993 Page(s):52 - 61
Digital Object Identifier 10.1109/2.211900
[Abstract](#) | Full Text: [PDF\(1732 KB\)](#) [IEEE JNL](#)
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 4. **Stack evaluation of arbitrary set-associative multiprocessor caches**

Yuguang Wu; Muntz, R.;
Parallel and Distributed Systems, IEEE Transactions on
Volume 6, Issue 9, Sept. 1995 Page(s):930 - 942
Digital Object Identifier 10.1109/71.466631
[Abstract](#) | Full Text: [PDF\(1240 KB\)](#) [IEEE JNL](#)
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 5. **Locality as a visualization tool**

Grimsrud, K.; Archibald, J.; Frost, R.; Nelson, B.;
Computers, IEEE Transactions on
Volume 45, Issue 11, Nov. 1996 Page(s):1319 - 1326
Digital Object Identifier 10.1109/12.544490
[Abstract](#) | Full Text: [PDF\(912 KB\)](#) [IEEE JNL](#)
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 6. **Compression-based program characterization for improving cache memory performance**

Phalke, V.; Gopinath, B.;
Computers, IEEE Transactions on
Volume 46, Issue 11, Nov. 1997 Page(s):1174 - 1186

- 7. Estimating neural networks-based algorithm for adaptive cache replacement**
Obaidat, M.S.; Khalid, H.;
[Systems, Man and Cybernetics, Part B, IEEE Transactions on](#)
Volume 28, Issue 4, Aug. 1998 Page(s):602 - 611
Digital Object Identifier 10.1109/3477.704299
[Abstract](#) | Full Text: [PDF\(304 KB\)](#) IEEE JNL
[Rights and Permissions](#)
- 8. Environment for PowerPC microarchitecture exploration**
Moudgil, M.; Wellman, J.-D.; Moreno, J.H.;
[Micro, IEEE](#)
Volume 19, Issue 3, May-June 1999 Page(s):15 - 25
Digital Object Identifier 10.1109/40.768496
[Abstract](#) | Full Text: [PDF\(1948 KB\)](#) IEEE JNL
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- 9. Lossless trace compression**
Johnson, E.E.; Jiheng Ha; Baqar Zaidi, M.;
[Computers, IEEE Transactions on](#)
Volume 50, Issue 2, Feb. 2001 Page(s):158 - 173
Digital Object Identifier 10.1109/12.908991
[Abstract](#) | Full Text: [PDF\(900 KB\)](#) IEEE JNL
[Rights and Permissions](#)
- 10. Low bit-rate efficient compression for seismic data**
Averbuch, A.Z.; Meyer, R.; Stromberg, J.-O.; Coifman, R.; Vassiliou, A.;
[Image Processing, IEEE Transactions on](#)
Volume 10, Issue 12, Dec. 2001 Page(s):1801 - 1814
Digital Object Identifier 10.1109/83.974565
[Abstract](#) | Full Text: [PDF\(332 KB\)](#) IEEE JNL
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- 11. Subject Index**
[Computers, IEEE Transactions on](#)
Volume 50, Issue 12, Dec. 2001 Page(s):1380 - 1388
Digital Object Identifier 10.1109/TC.2001.970577
[Abstract](#) | Full Text: [PDF\(70 KB\)](#) IEEE JNL
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- 12. Author Index**
[Computers, IEEE Transactions on](#)
Volume 50, Issue 12, Dec. 2001 Page(s):1377 - 1380
Digital Object Identifier 10.1109/TC.2001.970576
[Abstract](#) | Full Text: [PDF\(47 KB\)](#) IEEE JNL
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- 13. Study of an efficient simulation method**
Chang, Y.-R.;
[Computers and Digital Techniques, IEE Proceedings-](#)
Volume 146, Issue 5, Sept. 1999 Page(s):253 - 258
Digital Object Identifier 10.1049/ip-cdt:19990635
[Abstract](#) | Full Text: [PDF\(428 KB\)](#) IEE JNL
- 14. Heavy-tailed distribution of scene duration in VBR video**
Casilar, E.; Reyes, A.; Diaz-Estrella, A.; Sandoval, F.;
[Electronics Letters](#)
Volume 35, Issue 2, 21 Jan. 1999 Page(s):134 - 135
Digital Object Identifier 10.1049/el:19990102
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- 15. Method of correction for linear distortion of signals and application to DNA fingerprint data**
Menacer, M.; Woolfson, M.S.; Crowe, J.A.;
Electronics Letters
Volume 28, Issue 23, 5 Nov. 1992 Page(s):2126 - 2127
[Abstract](#) | Full Text: [PDF\(168 KB\)](#) IEE JNL
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- 16. New encapsulation modules for mm-wave GaAs transit-time devices**
Tschernitz, M.; Freyer, J.;
Electronics Letters
Volume 28, Issue 23, 5 Nov. 1992 Page(s):2125 - 2126
[Abstract](#) | Full Text: [PDF\(192 KB\)](#) IEE JNL
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- 17. Broadband Wavefront Reconstruction in Two-Dimensional Dispersive Space**
Boer, A.K.; Chambers, J.; Mason, I.M.; Legasse, P.E.;
Ultrasonics Symposium, 1976
1976 Page(s):160 - 162
[Abstract](#) | Full Text: [PDF\(272 KB\)](#) IEEE CNF
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- 18. Effect of Amplitude Limiting on Pulse Compression of Overlapping Linear Chirps**
Lafferl, J.; Kowatsch, M.; Seifert, F.J.;
Ultrasonics Symposium, 1981
1981 Page(s):231 - 235
[Abstract](#) | Full Text: [PDF\(392 KB\)](#) IEEE CNF
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- 19. Hardware-software co-design of embedded reconfigurable architectures**
Yanbing Li; Callahan, T.; Darnell, E.; Harr, R.; Kurkure, U.; Stockwood, J.;
Design Automation Conference, 2000. Proceedings 2000. 37th
June 5-9, 2000 Page(s):507 - 512
[Abstract](#) | Full Text: [PDF\(584 KB\)](#) IEEE CNF
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- 20. Reversible seismic data compression**
Meemong Lee; Yarlagadda, R.;
Acoustics, Speech, and Signal Processing, IEEE International Conference on ICASSP '82.
Volume 7, May 1982 Page(s):1870 - 1873
[Abstract](#) | Full Text: [PDF\(86 KB\)](#) IEEE CNF
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- 21. On the use of time compression for word-based recognition**
Gauvain, J.; Mariani, J.; Lienard, J.;
Acoustics, Speech, and Signal Processing, IEEE International Conference on ICASSP '83.
Volume 8, Apr 1983 Page(s):1029 - 1032
[Abstract](#) | Full Text: [PDF\(128 KB\)](#) IEEE CNF
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- 22. Compressing address traces with RECET**
Ahola, J.;
Workload Characterization, 2001. WWC-4. 2001 IEEE International Workshop on
2 Dec. 2001 Page(s):120 - 126
[Abstract](#) | Full Text: [PDF\(556 KB\)](#) IEEE CNF
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- 23. Iterative cache simulation of embedded CPUs with trace stripping**
Wu, Z.; Wolf, W.;
Hardware/Software Codesign, 1999. (CODES '99) Proceedings of the Seventh International Workshop on
3-5 May 1999 Page(s):95 - 99
Digital Object Identifier 10.1109/HSC.1999.777400
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24. Filter bank optimization for high-dimensional compression of pre-stack seismic data
Rosten, T.; Martinussen, V.A.; Ramstad, T.A.; Perkis, A.;
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Digital Object Identifier 10.1109/ICASSP.1999.757510
[Abstract](#) | Full Text: [PDF\(416 KB\)](#) IEEE CNF
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25. PDATS II: improved compression of address traces
Johnson, E.E.;
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10-12 Feb. 1999 Page(s):72 - 78
Digital Object Identifier 10.1109/PCCC.1999.749423
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Halbout, J.-M.; Tang, C.;
Quantum Electronics, IEEE Journal of
Volume 19, Issue 4, Apr 1983 Page(s):487 - 488
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 2. Lossless trace compression

Johnson, E.E.; Jiheng Ha; Baqar Zaidi, M.;
Computers, IEEE Transactions on
Volume 50, Issue 2, Feb. 2001 Page(s):158 - 173
Digital Object Identifier 10.1109/12.908991
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 3. Compressing address traces with RECET

Ahola, J.;
Workload Characterization, 2001. WWC-4. 2001 IEEE International Workshop on
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 4. PDATS II: improved compression of address traces

Johnson, E.E.;
Performance, Computing and Communications Conference, 1999. IPCCC '99. IEEE International
10-12 Feb. 1999 Page(s):72 - 78
Digital Object Identifier 10.1109/PCCC.1999.749423
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 5. Automatic ultrafast pulse compressor in chirped pulse amplification by FROG traces using fuzzy control technique

Furusawa, K.; Yabe, H.; Obara, M.;
Lasers and Electro-Optics Society Annual Meeting, 1998. LEOS '98. IEEE
Volume 1, 1-4 Dec. 1998 Page(s):138 - 139 vol.1
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[Rights and Permissions](#) 6. Compressing address trace data for cache simulations

Fox, A.; Grun, T.;
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- 7. **Taking into account access patterns irregularity when compressing address traces**
Hammami, O.;
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Digital Object Identifier 10.1109/SECON.1995.513060
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- 8. **Techniques for compressing program address traces**
Pleszkun, A.R.;
[Microarchitecture, 1994. MICRO-27. Proceedings of the 27th Annual International Symposium on](#)
30 Nov.-2 Dec. 1994 Page(s):32 - 39
Digital Object Identifier 10.1109/MICRO.1994.717407
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- 9. **PDATS Lossless Address Trace Compression For Reducing File Size And Access Time**
Johnson, E.E.; Jiheng Ha;
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12-15 Apr 1994 Page(s):213
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- 10. **Data compression for CAM with weighted double tracing method**
Fujimoto, M.; Kariya, K.;
[Industrial Electronics, Control and Instrumentation, 1994. IECON '94., 20th International Conference on](#)
Volume 2, 5-9 Sept. 1994 Page(s):1171 - 1175 vol.2
Digital Object Identifier 10.1109/IECON.1994.397957
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1. Lossless trace compression
Johnson, E.E.; Jiheng Ha; Baqar Zaidi, M.;
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Volume 50, Issue 2, Feb. 2001 Page(s):158 - 173
Digital Object Identifier 10.1109/12.908991
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2. Method of correction for linear distortion of signals and application to DNA fingerprint data
Menacer, M.; Woolfson, M.S.; Crowe, J.A.;
[Electronics Letters](#)
Volume 28, Issue 23, 5 Nov. 1992 Page(s):2126 - 2127
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3. Compressing address traces with RECET
Ahola, J.;
[Workload Characterization, 2001. WWC-4. 2001 IEEE International Workshop on](#)
2 Dec. 2001 Page(s):120 - 126
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4. PDATS II: improved compression of address traces
Johnson, E.E.;
[Performance, Computing and Communications Conference, 1999. IPCCC '99. IEEE International](#)
10-12 Feb. 1999 Page(s):72 - 78
Digital Object Identifier 10.1109/PCCC.1999.749423
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5. A method for improving the measurement data resolution of time-resolved spectroscopy (TRS) using adaptive pulse compression filter
Su Chang; Lin Fang; Ding Haishu; Chance, B.;
[Engineering in Medicine and Biology Society, 1998. Proceedings of the 20th Annual International Conference of the IEEE](#)
Volume 2, 29 Oct.-1 Nov. 1998 Page(s):994 - 997 vol.2
Digital Object Identifier 10.1109/EMBS.1998.745616
[AbstractPlus](#) | [Full Text: PDF\(324 KB\)](#) [IEEE CNF](#)
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6. Taking into account access patterns irregularity when compressing address traces
Hammami, O.;

- 7. Techniques for compressing program address traces**
Pleszkun, A.R.;
[Microarchitecture, 1994. MICRO-27. Proceedings of the 27th Annual International Symposium on](#)
30 Nov.-2 Dec. 1994 Page(s):32 - 39
Digital Object Identifier 10.1109/MICRO.1994.717407
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- 8. PDATS Lossless Address Trace Compression For Reducing File Size And Access Time**
Johnson, E.E.; Jiheng Ha;
[Computers and Communications, 1994. IEEE 13th Annual International Phoenix Conference on](#)
12-15 Apr 1994 Page(s):213
[AbstractPlus](#) | Full Text: [PDF\(676 KB\)](#) IEEE CNF
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- 9. Management of electrocardiographic tracings in a clinical departmental database**
Regalia, G.; Ravizza, P.; Bacchi, A.; Bossi, M.; Fiorini, R.; Dacquino, G.;
[Computers in Cardiology 1994](#)
25-28 Sept. 1994 Page(s):173 - 176
Digital Object Identifier 10.1109/CIC.1994.470221
[AbstractPlus](#) | Full Text: [PDF\(296 KB\)](#) IEEE CNF
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- 10. Deterministic delay bounds for VBR video in packet-switching networks: fundamental limits and practical trade-offs**
Wrege, D.E.; Knightly, E.W.; Hui Zhang; Liebeherr, J.;
[Networking, IEEE/ACM Transactions on](#)
Volume 4, Issue 3, June 1996 Page(s):352 - 362
Digital Object Identifier 10.1109/90.502234
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(1044 KB\)](#) IEEE JNL
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- 11. Admission control for statistical QoS: theory and practice**
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Y Li, T Callahan, E Darnell, R Harr, U Kurkure, J ... - Design Automation Conference (DAC), 2000 - doi.ieeecomputersociety.org

... Embedded CPU **On chip** SRAM / Caches ... Loop **trace compression** not only saves storage
 space, but more importantly, the compact representation allows fast traversing ...

[Cited by 106](#) - [Web Search](#) - [BL Direct](#)

An object code **compression** approach to embedded processors - group of 2 »

Y Yoshida, BY Song, H Okuhata, T Onoye, I ... - Proceedings of the 1997 international symposium on Low power ..., 1997 -
[portal.acm.org](#)

... 1, where specific functional units, **on-chip** memories, etc ... on these considerations,
 an object **compression** scheme is ... embedded program of m-bitwidth, **trace** it to ...

[Cited by 45](#) - [Web Search](#)

Address **compression** through base register caching - group of 2 »

A Park, M Farrens - Proceedings of the 23rd annual workshop and symposium on ..., 1990 - [portal.acm.org](#)

... How much address **compression** is practical ... taken from simulations using the composite

ATUM **trace** with system ... simulations to examine how an **on-chip** cache affects ...

[Cited by 10](#) - [Web Search](#)

An analysis of the information content of address and data reference streams

JC Becker, A Park - Proceedings of the 1993 ACM SIGMETRICS conference on ..., 1993 - [portal.acm.org](#)

... and performance gains which are attained by **on-chip** Harvard architectures in ... Table

6: Data stream **compression** achieved by our scheme **trace#com-** instruction ...

[Cited by 4](#) - [Web Search](#) - [BL Direct](#)

Reducing power in high-performance microprocessors - group of 10 »

V Tiwari, D Singh, S Rajgopal, G Mehta, R Patel, F ... - Proceedings of the 35th annual conference on Design ..., 1998 -
[doi.ieeecomputersociety.org](#)

... In addition, multiple **on-chip** units and power down ... The selection/**compression** must
 ensure that the characteristics of an application **trace** that track a ...

[Cited by 145](#) - [Web Search](#) - [BL Direct](#)

A selective compressed memory system by on-line data decompressing - group of 4 »

JS Lee, WK Hong, SD Kim - EUROMICRO Conference, 1999. Proceedings. 25th, 1999 - doi.ieeecomputersociety.org

... using Shade Tool , which can **trace** both the ... file is generated after the

compression/decompression processes ... the SCMS simulator designed for the **on-chip** 2 ...

[Cited by 3](#) - [Web Search](#)

Address tracing for parallel machines - group of 7 »

CB Stunkel, B Janssens, WK Fuchs - Computer, 1991 - doi.ieeecs.org

... performance microprocessors available, the trend toward **on-chip** caches in ... of address
 traces, concurrent simulation with tracing, **trace compression**, and **trace** ...

[Cited by 33](#) - [Web Search](#)

Event monitoring in highly complex hardware systems - group of 4 »

T Buechner, R Fritz, P Guenther, M Helms, KD Lamb, ... - IBM J. RES. DEV, 1999 - research.ibm.com

... there is one **compression** unit that generates a unique signature for the path the
 operation has followed. The tracing unit has its own 1KB **on-chip** trace array. ...

[Collecting address traces from parallel computers - group of 2 »](#)

CB Stunkel, B Janssens, WK Fuchs - System Sciences, 1991. Proceedings of the Twenty-Fourth ... , 1991 - ieeexplore.ieee.org

... the trend toward **on-chip** caches in these processors will limit the effectiveness

of hardware-based tracing techniques. The completeness of the **trace** is also ...

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[PDATS: Lossless Address Trace Compression for Reducing File..](#) - Johnson, Ha (1994) (Correct) (21 citations)
this paper we present an information-lossless **trace compression** scheme that can reduce both storage space
The following sections present the PDATS **trace compression** scheme and an evaluation of its
tracebase.nmsu.edu/pub/pubs/pdats.ps.Z

[Monitoring Very High Speed Links](#) - Iannaccone, Diot, Graham, McKeown (2001) (Correct) (15 citations)
to be used in conjunction with a flow-based **trace compression**. In this document, we discuss the
www.aciri.org/vern/imw-2001/imw2001-papers/63.ps.gz

[Techniques for Cache and Memory Simulation Using Address..](#) - Holliday (1990) (Correct) (9 citations)
of the large size of traces. Techniques for **trace compression** and trace reduction have been developed.
inline simulation section. In the second, **trace compression** decreases the size of the trace in storage,
large size of traces. Techniques for **trace compression** and trace reduction have been developed. Trace
ftp.cs.duke.edu/pub/dist/papers/NUMATic/ijcs91.ps.Z

[Trace Reduction for Virtual Memory Simulations](#) - Scott Kaplan Yannis (2004) (Correct) (3 citations)
Johnson and J. Ha, PDATS: Lossless Address Trace Compression for Reducing File Size and Access Time"
2.1 Overview of Related Work Like all data **compression**, trace reduction techniques are divided into
www.cs.amherst.edu/~sfkaplan/courses/spring-2004/cs40/papers/./KSW:TRVMS.pdf

[SIGMA: A Simulator Infrastructure to Guide Memory Analysis](#) - DeRose, Ekanadham.. (2002) (Correct) (3 citations)
the entire execution of the program. 2.2 **Trace Compression** Loops in programs provide an excellent
375.9 2,073.3 477.6 4 4.34 Table 1: **Trace compression** statistics 2.4 Source Code and Data
www.sc2002.org/paperpdfs/pap.pap191.pdf

[ATOM Reference Manual](#) - December Digital Equipment (1993) (Correct) (3 citations)
traces by modifying microcode. ATUM performs **trace compression** and saves the trace in a file that is
www.partner.digital.com/www-swdev/files/DECOSF1/Docs/Other/ATOM/ref.ps

[PDATS II: Improved Compression of Address Traces](#) - Johnson (1999) (Correct) (2 citations)
and instruction traces. The PDATS family of **trace compression** techniques achieves trace coding densities
lost in the process. The two lossless address **trace compression** schemes reported in the literature are
tracebase.nmsu.edu/pub/pubs/pdats2.pdf

[Detecting Memory Performance Bottlenecks via Binary Rewriting](#) - Marathe, Mueller (2002) (Correct) (1 citation)
CFG Mutator (Controller) Expanded View **Trace Compression** Routines (Shared Library)
moss.csc.ncsu.edu/~mueller/ftp/pub/mueller/papers/wbt02.ps.gz

[RATCHET: Real-time Address Trace Compression Hardware for..](#) - Colleen Schieber And (1994) (Correct) (1 citation)
4, April 1994 22 RATCHET: Real-time Address Trace Compression Hardware for Extended Traces Colleen D.
ratio results have been reported for the **trace compression** methods discussed above. Stunkel and Fuchs
tracebase.nmsu.edu/pub/pubs/ratchet.pdf

[A Comparison Of Address Translation Mechanisms For..](#) - Tuch (2002) (Correct)
. 51 3.2.2 **Trace compression**.
Experimental Method 54 .Arm Sys Brk 3.2.2 **Trace Compression** Each Memory Reference Required 5 Bytes To
www.disy.cse.unsw.edu.au/theses_public/02/htuch.ps.gz

[Custom Instruction filter Cache Synthesis for Low-Power ..](#) - Kugan Vivekanandarajah .. (Correct)
on reducing the time required by using **trace compression** and /or simulating multiple
configurations[20, 21] in a single pass. In **trace compression**, a reduced trace is obtained which
www.ntu.edu.sg/home5/pm2096207/rsp.pdf

[Predicting Hierarchical Phases in Program Data Behavior](#) - Xipeng Shen Yutao (Correct)
among recent ones are memory management, **trace compression** [21] and the file caching for PCs, servers

including better page replacement and **trace compression** [21] Zhou et al. 25] and Jiang and Zhang
www.cs.rochester.edu/u/xshen/Publications/TR824.pdf

A Distributed Architecture for Dynamic Analyses on.. - Giuliano Antoniol And (2004) (Correct)
in our model. A non-loss approach to **trace compression**, oriented to performance analysis, was
www.rcost.unisannio.it/mdipenta/papers/csmr2004.pdf

Citcat: Constructing Instruction Traces From Cache-Filtered.. - Rose (1999) (Correct)
as an extremely efficient, lossless **trace compression** algorithm. ACKNOWLEDGMENTS Thanks to
34 5.3. **Trace Compression**.
pel.cs.byu.edu/pubs/rose99/rose99.pdf

VPC3: A Fast and Effective Trace-Compression Algorithm - Martin Burtscher Computer (Correct)
VPC3: A Fast and Effective **Trace-Compression** Algorithm Martin Burtscher Computer
Design, Experimentation. Keywords **Trace compression**, predictor-based **compression**, **trace files**.
Keywords **Trace compression**, predictor-based **compression**, **trace files**. 1. INTRODUCTION Program execution
www.csl.cornell.edu/~burtscher/papers/sigm04.pdf

Unknown - (2002) (Correct)

.8 4.3 **Trace Compression**.
of interpretation and translation. 4.3 **Trace Compression** Using the Soot [25] bytecode
www.sable.mcgill.ca/step/tr/sable-tr-2002-7.ps.gz

N-Tuple Compression: - Novel Method For (Correct)

and trace caches. A novel method for lossless **trace compression**, which can be applied to both ASCII and
trace-driven simulation, branch prediction, **trace compression**. 1. INTRODUCTION The dynamic branch
30 times for some benchmarks and 8-tuple **compression**. **Trace** access time is also reduced. Finally, we
www.ece.uah.edu/~milenka/docs/milenkovic_pdcs03.pdf

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1 Techniques for compressing program address traces

Andrew R. Pleszkun

 November 1994 **Proceedings of the 27th annual international symposium on Microarchitecture**

Publisher: ACM Press

 Full text available: [pdf\(931.63 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

In this paper a technique for generating consistent, reproducible traces with about an order of magnitude better compression than standard general-purpose compression programs is described. With this approach, the trace is read once, an intermediate form is generated and then read as the input to the second pass over the address stream. No program source code is required, and this technique will work on address streams that include OS calls. As a result of the way the address trace is encoded ...

Keywords: compression, trace generation


2 RATCHET: real-time address trace compression hardware for extended traces

Colleen D. Schieber, Eric E. Johnson

 April 1994 **ACM SIGMETRICS Performance Evaluation Review**, Volume 21 Issue 3-4

Publisher: ACM Press

 Full text available: [pdf\(783.24 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

The address traces used in computer architecture research are commonly generated using software techniques that introduce time dilations of an order of magnitude or more. Such techniques may also omit classes of memory references that are important for accurate models of computer systems, such as instruction prefetches, operating system references, and interrupt activity. We describe a technique for capturing all classes of references in real time. RATCHET employs trace filtering hardware to reduce ...



3 Address trace compression through loop detection and reduction

E. N. Elnozahy

 May 1999 **ACM SIGMETRICS Performance Evaluation Review, Proceedings of the 1999 ACM SIGMETRICS international conference on Measurement and modeling of computer systems SIGMETRICS '99**, Volume 27 Issue 1

Publisher: ACM Press

 Full text available: [pdf\(226.94 KB\)](#) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)
Keywords: address traces, compression, control flow analysis, traces

4 Mache: no-loss trace compaction

 A. D. Samples

April 1989 **ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 1989 ACM SIGMETRICS international conference on Measurement and modeling of computer systems SIGMETRICS '89**, Volume 17 Issue 1

Publisher: ACM Press

Full text available:  pdf(798.23 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Execution traces can be significantly compressed using their referencing locality. A simple observation leads to a technique capable of compressing execution traces by an order of magnitude; instruction-only traces are compressed by two orders of magnitude. This technique is unlike previously reported trace compression techniques in that it compresses without loss of information and, therefore, does not affect trace-driven simulation time or accuracy.

5 Designing a trace format for heap allocation events

 Trishul Chilimbi, Richard Jones, Benjamin Zorn

October 2000 **ACM SIGPLAN Notices , Proceedings of the 2nd international symposium on Memory management ISMM '00**, Volume 36 Issue 1

Publisher: ACM Press

Full text available:  pdf(1.53 MB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Dynamic storage allocation continues to play an important role in the performance and correctness of systems ranging from user productivity software to high-performance servers. While algorithms for dynamic storage allocation have been studied for decades, much of the literature is based on measuring the performance of benchmark programs unrepresentative of many important allocation-intensive workloads. Furthermore, to date no standard has emerged or been proposed for publishing and exchangin ...

6 Potential benefits of delta encoding and data compression for HTTP

 Jeffrey C. Mogul, Fred Douglis, Anja Feldmann, Balachander Krishnamurthy

October 1997 **ACM SIGCOMM Computer Comm unication Review , Proceedings of the ACM SIGCOMM '97 conference on Applications, technologies, architectures, and protocols for computer communication SIGCOMM '97**, Volume 27 Issue 4

Publisher: ACM Press

Full text available:  pdf(2.00 MB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Caching in the World Wide Web currently follows a naive model, which assumes that resources are referenced many times between changes. The model also provides no way to update a cache entry if a resource does change, except by transferring the resource's entire new value. Several previous papers have proposed updating cache entries by transferring only the differences, or "delta," between the cached entry and the current value.In this paper, we make use of dynamic traces of the full contents of ...

7 Low-loss TCP/IP header compression for wireless networks

Mikael Degermark, Mathias Engan, Björn Nordgren, Stephen Pink

October 1997 **Wireless Networks**, Volume 3 Issue 5

Publisher: Kluwer Academic Publishers

Full text available:  pdf(534.08 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Wireless is becoming a popular way to connect mobile computers to the Internet and other networks. The bandwidth of wireless links will probably always be limited due to properties of the physical medium and regulatory limits on the use of frequencies for radio communication. Therefore, it is necessary for network protocols to utilize the available bandwidth efficiently. Headers of IP packets are growing and the bandwidth required for transmitting headers is increasing. With the coming of I ...

8 Low-loss TCP/IP header compression for wireless networks

Mikael Degermark, Mathias Engan, Björn Nordgren, Stephen Pink

Publisher: ACM Press

Full text available: [pdf\(1.51 MB\)](#)

Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

9 Trace reduction for virtual memory simulations

Scott F. Kaplan, Yannis Smaragdakis, Paul R. Wilson

May 1999 **ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 1999 ACM SIGMETRICS international conference on Measurement and modeling of computer systems SIGMETRICS '99**, Volume 27 Issue 1

Publisher: ACM Press

Full text available: [pdf\(1.44 MB\)](#)

Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

10 Trace-driven memory simulation: a survey

Richard A. Uhlig, Trevor N. Mudge

June 1997 **ACM Computing Surveys (CSUR)**, Volume 29 Issue 2

Publisher: ACM Press

Full text available: [pdf\(636.11 KB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#), [review](#)

As the gap between processor and memory speeds continues to widen, methods for evaluating memory system designs before they are implemented in hardware are becoming increasingly important. One such method, trace-driven memory simulation, has been the subject of intense interest among researchers and has, as a result, enjoyed rapid development and substantial improvements during the past decade. This article surveys and analyzes these developments by establishing criteria for evaluating trac ...

Keywords: TLBs, caches, memory management, memory simulation, trace-driven simulation

11 Blocking: exploiting spatial locality for trace compaction

Anant Agarwal, Minor Huffman

April 1990 **ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 1990 ACM SIGMETRICS conference on Measurement and modeling of computer systems SIGMETRICS '90**, Volume 18 Issue 1

Publisher: ACM Press

Full text available: [pdf\(1.01 MB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Trace-driven simulation is a popular method of estimating the performance of cache memories, translation lookaside buffers, and paging schemes. Because the cost of trace-driven simulation is directly proportional to trace length, reducing the number of references in the trace significantly impacts simulation time. This paper concentrates on trace driven simulation for cache miss rate analysis. Previous schemes, such as cache filtering, exploited temporal locality for compressing traces and ...

12 Completeness and incompleteness of trace-based network proof systems

J. Widom, D. Gries, F. B. Schneider

October 1987 **Proceedings of the 14th ACM SIGACT-SIGPLAN symposium on Principles of programming languages**

Publisher: ACM Press

Full text available: [pdf\(1.30 MB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Most trace-based proof systems for networks of processes are known to be incomplete. Extensions to achieve completeness are generally complicated and cumbersome. In this paper, a simple trace logic is defined and two examples are presented to show its inherent incompleteness. Surprisingly, both examples consist of only one process, indicating that network composition is not a cause of incompleteness. Axioms necessary

and sufficient for the relative completeness of a trace logic are then pre ...

13 Optimal tracing and incremental reexecution for debugging long-running programs 
Robert H. B. Netzer, Mark H. Weaver
June 1994 **ACM SIGPLAN Notices**, **Proceedings of the ACM SIGPLAN 1994 conference on Programming language design and implementation PLDI '94**, Volume 29 Issue 6
Publisher: ACM Press
Full text available:  [pdf\(1.34 MB\)](#) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

14 Modeling and simulation of self-similar variable bit rate compressed video: a unified approach 
Changcheng Huang, Michael Devetsikiotis, Ioannis Lambadaris, A. Roger Kaye
October 1995 **ACM SIGCOMM Computer Communication Review**, **Proceedings of the conference on Applications, technologies, architectures, and protocols for computer communication SIGCOMM '95**, Volume 25 Issue 4

Publisher: ACM Press
Full text available:  [pdf\(1.06 MB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Variable bit rate (VBR) compressed video is expected to become one of the major loading factors in high-speed packet networks such as ATM-based B-ISDN. However, recent measurements based on long empirical traces (complete movies) revealed that VBR video traffic possesses *self-similar* (or *fractal*) characteristics, meaning that the dependence in the traffic stream lasts much longer than traditional models can capture. In this paper, we present a unified approach which, in addition to ...

15 Multi-layer tracing of TCP over a reliable wireless link 
Reiner Ludwig, Bela Rathonyi, Almudena Konrad, Kimberly Oden, Anthony Joseph
May 1999 **ACM SIGMETRICS Performance Evaluation Review**, **Proceedings of the 1999 ACM SIGMETRICS international conference on Measurement and modeling of computer systems SIGMETRICS '99**, Volume 27 Issue 1
Publisher: ACM Press
Full text available:  [pdf\(1.37 MB\)](#) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

Keywords: GSM, TCP, measurement tools, wireless

16 Path-based next trace prediction 
Quinn Jacobson, Eric Rotenberg, James E. Smith
December 1997 **Proceedings of the 30th annual ACM/IEEE international symposium on Microarchitecture**
Publisher: IEEE Computer Society
Full text available:   [pdf\(1.15 MB\)](#) [Publisher Site](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

The trace cache has been proposed as a mechanism for providing increased fetch bandwidth by allowing the processor to fetch across multiple branches in a single cycle. But to date predicting multiple branches per cycle has meant paying a penalty in prediction accuracy. We propose a next trace predictor that treats the traces as basic units and explicitly predicts sequences of traces. The predictor collects histories of trace sequences (paths) and makes predictions based on these histories. The b ...

Keywords: Trace Cache, Next Trace Prediction, Multiple Branch Prediction, Return History Stack, Path-Based Prediction

17 Analysis of branch prediction via data compression 
I-Cheng K. Chen, John T. Coffey, Trevor N. Mudge

Publisher: ACM Press

Full text available:  [pdf\(930.57 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Branch prediction is an important mechanism in modern microprocessor design. The focus of research in this area has been on designing new branch prediction schemes. In contrast, very few studies address the theoretical basis behind these prediction schemes. Knowing this theoretical basis helps us to evaluate how good a prediction scheme is and how much we can expect to improve its accuracy. In this paper, we apply techniques from data compression to establish a theoretical basis for branch predic ...

18 On management of free space in compressed memory systems 

 Peter A. Franaszek, Philip Heidelberger, Michael Wazlowski
May 1999 **ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 1999 ACM SIGMETRICS international conference on Measurement and modeling of computer systems SIGMETRICS '99**, Volume 27 Issue 1

Publisher: ACM Press

Full text available:  [pdf\(1.16 MB\)](#) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

19 Branch prediction based on universal data compression algorithms 

 Eitan Federovsky, Meir Feder, Sholomo Weiss
April 1998 **ACM SIGARCH Computer Architecture News , Proceedings of the 25th annual international symposium on Computer architecture ISCA '98**, Volume 26 Issue 3

Publisher: IEEE Computer Society, ACM Press

Full text available:  [pdf\(987.72 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)
 [Publisher Site](#)

Data compression and prediction are closely related. Thus prediction methods based on data compression algorithms have been suggested for the branch prediction problem. In this work we consider two universal compression algorithms: prediction by partial matching (PPM), and a recently developed method, context tree weighting (CTW). We describe the prediction algorithms induced by these methods. We also suggest adaptive algorithms --- variations of the basic methods that attempt to fit limited mem ...

20 Alternative fetch and issue policies for the trace cache fetch mechanism 

Daniel Holmes Friendly, Sanjay Jeram Patel, Yale N. Patt
December 1997 **Proceedings of the 30th annual ACM/IEEE international symposium on Microarchitecture**

Publisher: IEEE Computer Society

Full text available:   [pdf\(1.16 MB\)](#) [Publisher Site](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

The increasing widths of superscalar processors are placing greater demands upon the fetch mechanism. The trace cache meets these demands by placing logically contiguous instructions in physically contiguous storage. It is capable of supplying multiple fetch blocks each cycle. In this paper we examine two fetch and issue techniques, partial matching and inactive issue, that improve the overall performance of the trace cache by improving the effective fetch rate. We show that for the SPECint95 be ...

Keywords: high bandwidth fetch mechanisms, trace cache, wide issue machines, speculative execution, partial matching, inactive issue

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